ABSTRACT OF THE DISCLOSURE

A method for designing a semiconductor device in which dummy pattern density and design pattern density are equalized on the entire semiconductor chip. A layout pattern for a layout layer in a semiconductor device is divided into divided areas (step S1). A dummy pattern is inserted between design patterns in the divided areas obtained by dividing the layout pattern (step S2). Dummy pattern density and design pattern density in each divided area are calculated (step S3). Pattern rules for a dummy pattern in each divided area are changed so that the dummy pattern density and the design pattern density will be desired values (step S4).